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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,430	10/23/2003	Roger W. Lindsay	400.263US01	8403

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,430	LINDSAY, ROGER W.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/25/2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 and 42-62 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 42-62 is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-13 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen (U.S. 20050040444).

Cohen discloses a semiconductor device with

(1); (9) forming a source slot and a drain contact region at opposite ends of a NAND string disposed on a substrate (1, 2) of the memory array using a single mask, the NAND string comprising a plurality of memory cells connected in series between a source select gate (18A) and a drain select gate (18C), wherein a portion of the drain

contact region (20) is formed directly over the drain select gate (18C) and wherein the single mask defines areas for exposing the substrate (1, 2) (see Figures 18-19);

(2) further comprising, before forming the source slot and the drain contact region, forming a dielectric layer on the substrate, the NAND string, and source and drain select gates (see Figures 18-19);

(3) further comprising aligning the drain contact region to a sidewall of the drain select gate (see Figures 18-19);

(4) wherein forming the source slot and the drain contact region comprises removing the dielectric layer from the substrate (see Figures 18-19);

(5) further comprising forming a source line in the source slot and a drain contact in the drain contact region (see Figures 18-19);

(6) wherein the source slot and the drain contact region are formed substantially simultaneously (see Figures 18-19);

(7) further comprising forming a bit line contact in contact with the drain contact (see Figures 18-19);

(8) further comprising aligning the source slot to a sidewall of the source select gate (see Figures 18-19);

(10) wherein forming the source slot and the drain contact region comprises removing the dielectric layer from the substrate (see Figures 18-19);

(11) further comprising forming a source line in the source slot and a drain contact in the drain contact region (see Figures 18-19);

(12) further comprising forming a bit line contact in contact with the drain contact (see Figures 18-19);

(13) wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate (see Figures 18-19);

(17) wherein self aligning the drain contact region to the dielectric layer on the drain select gate further comprises self aligning the drain contact region to another drain select gate connected to another NAND string (see Figures 18-19).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (U.S. 20050040444).

Cohen discloses the claimed invention except for selecting specifically material for the dielectric layer and the bulk insulation layer. It would have been obvious to one

having ordinary skill in the art at the time the invention was made to select the best material to meet its purpose, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claims 18-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (U.S. 20050040444) in view of Sakui et al. (U.S. 6,411,548 B1).

Cohen discloses a semiconductor device with

(18); (25) forming a dielectric layer on a substrate, a NAND string disposed on the substrate, and source and drain select gates respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, the NAND string comprising a plurality of memory cells connected in series (see Figures 18-19).

Cohen teaches the above outlined features except for forming a bulk insulation layer on the dielectric layer; forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate. wherein a portion of the drain contact region directly overlies the drain select gate; removing the dielectric layer from the substrate within the source slot and drain contact region; forming a source line in the source slot and a drain contact in the drain contact region; forming a bit line contact in contact with the drain contact.

However, Sakui discloses a semiconductor device with **(18); (25)**....forming a bulk insulation layer on the dielectric layer; forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate. wherein a portion of the drain contact region directly overlies the drain select gate; removing the dielectric layer from the substrate within the source slot and drain contact region; forming a source line in the source slot and a drain contact in the drain contact region; forming a bit line contact in contact with the drain contact (see column 12, lines 1-65; column 13, lines 5-67 and column 14, lines 1-65. Figures 12-14); **(19)** wherein forming the source line in the source slot and the drain contact in the drain contact region, comprises: forming a polysilicon plug in the source slot in contact with the substrate and a polysilicon plug in the drain contact region in contact with the substrate; forming an electrically conducting plug on the polysilicon plug in the source slot and on the polysilicon plug in the drain contact region (see Figures 12-14); **(20)** wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate (see Figures 12-14); **(21)** further comprising forming an interlayer dielectric on the bulk insulation layer and on the source line and the drain contact before forming the bit line contact (see Figures 12-14); **(22)** wherein the drain contact passes through the interlayer dielectric (see Figures 12-14); **(23)** wherein the drain contact comprises a head connected substantially perpendicularly to a stem, wherein the bit line contact is formed in contact with the head

(see Figures 12-14); **(24)** wherein the head overlies the dielectric layer on the drain select gate and is aligned with the drain select gate, and the stem overlies the polysilicon plug (see Figures 12-14); **(26)** wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate (see Figures 12-14); **(27)** further comprising forming a metal layer on the interlayer dielectric in electrical contact with the bit line contact (see Figures 12-14); **(28)** further comprising forming a bit line from the metal layer so that the bit line is in electrical contact with the bit line contact (see Figures 12-14). Therefore, it It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Cohen (accordance with the teaching of Sakui). Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the semiconductor structure.

Allowable Subject Matter

Claims 42-62 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined claims define over the prior art. The cited prior art does not disclose or suggest a semiconductor memory transistor inter alia the limitations "...forming a drain select gate overlying the substrate and adjacent a drain of a last floating-gate transistor of the plurality of serially-connected floating-gate transistors, a source of the drain select gate coupled to a drain of the last floating-gate transistor; forming a first layer of

dielectric material overlying the source select gate, the NAND string, the drain select gate, and exposed surfaces of the substrate adjacent the source and drain select gates; forming a second layer of dielectric material overlying the first layer of dielectric material, wherein the second layer of dielectric material comprises a dielectric material different from the first layer of dielectric material; patterning the second layer of dielectric material to expose portions of the first layer of dielectric material adjacent the source select gate, adjacent the drain select gate and overlying the drain select gate to thereby define a source slot and a drain contact region substantially concurrently; removing exposed portions of the first layer of dielectric material adjacent the source select gate and adjacent the drain select gate, thereby exposing portions of the substrate adjacent the source select gate and the drain select; forming a first layer of conductive material overlying the second layer of dielectric material and in contact with the exposed portions of the substrate; removing an upper portion of the first layer of conductive material to recess it below a surface of the second layer of dielectric material, thereby leaving a first portion of the first layer of conductive material in the source slot and a second portion of the first layer of conductive material in the drain contact region; substantially concurrently forming a source line coupled to the first portion of the first layer of conductive material and a drain contact coupled to the second portion of the first layer of conductive material; forming a third layer of dielectric material overlying the second layer of dielectric material, the source line, and the drain contact; forming a bit line contact through the third layer of dielectric material and coupled to a portion of the drain contact overlying the drain select gate..."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
August 4, 2006